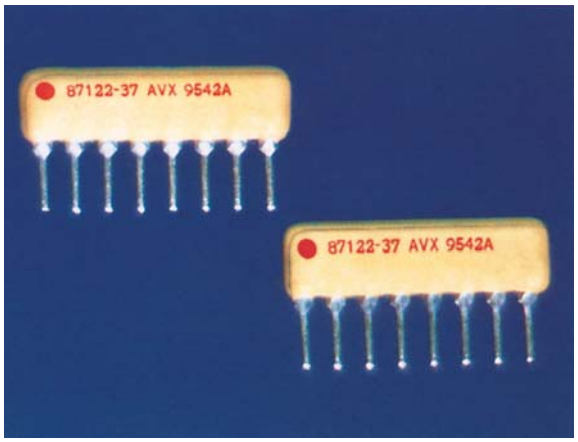
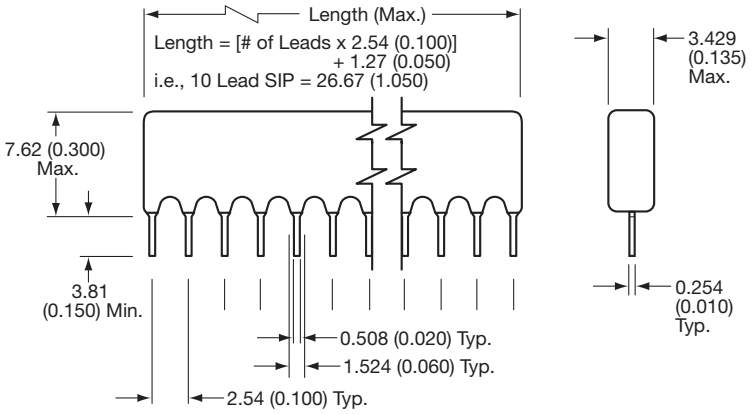
Single-In-Line Packages (SIP)

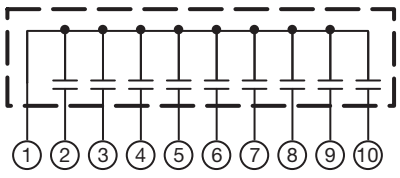
Capacitor Arrays



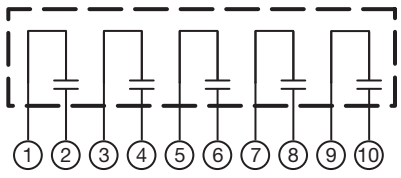
SIP-style, MLC ceramic capacitor arrays are Single-In-Line, conformally coated packages. These capacitor networks incorporate multiple capacitors into a single substrate and, therefore, offer excellent TC tracking. The utilization of SIP capacitor arrays minimizes board real estate and reduces component count in the assembly. Various circuit configurations and capacitance/voltage values are available.

Dimensions in millimeters (inches)

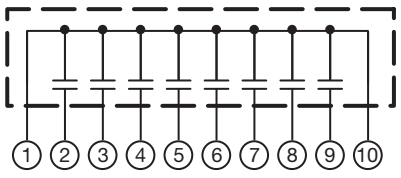




CIRCUIT CONFIGURATION "A"
ONE END LEAD GROUND



CIRCUIT CONFIGURATION "B"
ADJACENT LEAD PAIR CAPS



CIRCUIT CONFIGURATION "C"
BOTH END LEADS GROUND

Single-In-Line Packages (SIP)

Capacitor Arrays

HOW TO ORDER

SP	A	1	1	A	561	K	A	A
AVX Style	**Circuit** See page 139 (A, B, C)	**Lead Style**	**Voltage** 50V = 5 100V = 1	**Temperature Coefficient** C0G = A X7R = C Z5U = E	**Capacitance Code** (2 significant digits + no. of zero) 10 pF = 100 100 pF = 101 1,000 pF = 102 22,000 pF = 223 220,000 pF = 224 1 µF = 105 10 µF = 106 100 µF = 107	**Capacitance Tolerance** C0G: K = ±10% M = ±20% X7R: K = ±10% M = ±20% Z = +80%,-20% Z5U: M = ±20% Z = +80%,-20% P = GMV (+100,-0%)	**Test Level** A = Standard	**Number of Leads** 2 = 2 3 = 3 4 = 4 5 = 5 6 = 6 7 = 7 8 = 8 9 = 9 A = 10 B = 11 C = 12 D = 13 E = 14

*For dimensions, voltages, or capacitance values not specified, please contact factory.

Not RoHS Compliant

Maximum Capacitance*		
	50V	**100V**
C0G	2200 pF	1500 pF
X7R	0.10 µF	0.10 µF
Z5U	0.39 µF	0.10 µF

AVX IS QUALIFIED TO THE FOLLOWING DSCC DRAWINGS

SPECIFICATION #	DESCRIPTION	CIRCUIT	LEADS	CAPACITANCE RANGE
87112	BX-100 VDC	A	8	1000 pF - 0.1 µF
87116	C0G-100 VDC	A	8	10 pF - 820 pF
87119	BX-100 VDC	C	10	1000 pF - 0.1 µF
87120	C0G-100 VDC	C	10	10 pF - 1000 pF
87122	BX-100 VDC	B	8	1000 pF - 0.1 µF
88019	BX-100 VDC	A	10	1000 pF - 0.1 µF
89086	C0G-100 VDC	B	8	10 pF - 820 pF